Technological Roadmap For Low-Power Commercial Off-The-Shelf (COTS) Parts

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Risk Assessment of Low-Power Space Electronics
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Note

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This report presents the results of Phase 1 of the RTOP "Risk Assessment of Low-Power Space Electronics". Phases 2 and 3 will deal with the identification of failure mechanisms, their risk assessment, and measures for their mitigation.

Content

Section 1: Introduction

COTS

The last decade of the 20th century has brought revolutionary changes in the use of electronics in virtually all aspects of life. The external driving forces were the end of the cold war and the necessity to cut government spending. Internal forces were huge consumer markets created by electronic applications like personal computers and communications equipment.

The legislative groundwork for a reform of defense procurement was completed with passage of the Federal Acquisition Streamlining Act (FASTA) of 1994 [1]. Commercial off-the-shelf acquisitions on the parts level were encouraged for the following benefits: Commercial industry today paces technological change in many areas, especially in electronics. Mass-produced commercial parts are more cost effective in acquisition and maintenance. Relief from regulation through MIL standards saves about 18% of contractor's value. Acquisition cycle times are reduced from typical 15 years in the old military paradigm to 3-4 years.

NASA followed this trend soon with the now famous slogan "faster, cheaper, better".

Low-Power Electronics

Low-power electronics is a prime example of commercially driven technology. Commercial interest in components with low power consumption stems mainly from two applications:

1. Portable computing and communication devices run on batteries with limited charge capacity. Battery weight is also an important factor.
2. Faster processors require a higher degree of compactness. This concentrates dissipated power in a small volume, which is difficult to cool. In order to avoid high temperatures, power dissipation must be lowered.

3. Convection cooling may not be available due to lack of or significant reduction of atmospheric pressure.

Power loss in digital integrated circuits (ICs) has been attributed to the following mechanisms:

1. node charging
2. short circuit (crow-bar) current
3. leakage current

Dynamic power dissipation is experienced in digital ICs during switching a node n from one state to the other. Node charging rises linearly with the switching frequency f_n , the load capacitance for the node C_n, and with the square of the supply voltage V_{DD} (assuming swing voltage $V_s = V_{DD}$):[2]

$$P_{L,n} = f_n C_n V_{DD}^2 . \quad (1)$$

For a CMOS inverter with a junction capacitance $C_{j,n}$ driving other inverters with a total gate capacitance $C_{g,n}$ through wires with a total capacitance $C_{w,n}$, the node capacitance is:

$$C_n = C_{j,n} + C_{g,n} + C_{w,n} . \quad (2)$$

The short-circuit or crowbar current flows from V_{DD} to ground during switching when both transistors of the inverter are conducting. The dissipated power is[3]

$$P_{C,n} \mu f_n t_n [V_{DD}(1 - 2v)]^{a+1}, \quad (3)$$

where t_n is the node transition time, $v = V_t/V_{DD} < ½$, and $2 > \alpha \rightarrow 1$ for short channels.

The loss due to subthreshold leakage of the off-transistor is[4]

$$P_L = V_{DD} I_0 \acute{}10^{-x}; \; x = -(V_t/S), \quad (4)$$

where V_t is the threshold voltage, S the subthreshold slope, and I_0 the current for the gate voltage equal to V_t .

Since the contributions from Eqs. (3) and (4) are very small in comparison to that of Eq.

4. introducing interlevel dielectrics and substrate (SOI) with low permittivity, planarize metallization → lower $C_{w,n}$

Details of these measures will be outlined in detail in the second Section.

The power optimization of portable communications equipment requires some different considerations in the radio-frequency (RF) parts. Here noise, linearity, and conversion efficiency play the main roles[5]. GaAs-MESFETs have been the main technology for portable communications. However, silicon-based devices have recently made so much progress into the 900-MHz range that they have started to displace GaAs-based devices.

Details of trends for low-power RF technology will be presented in the third Section.

Section 2: Digital Technology

The near-term technology of choice is considered silicon bulk CMOS with Silicon-On-Insulator (SOI) substrates likely to make in-roads mid-term.

Parameter Targets

For digital technology very detailed roadmaps have been developed by the Semiconductor Industry Association (SIA) and published in 1994 [6] and 1997 [7]. These maps set technology generations characterized by minimum feature sizes. While the 1994 map projected the introduction of a new generation characterized by DRAM feature size and capacity following Moore's law every 3 years, the 1997 map projects new feature sizes for DRAMs *and* MPUs on 2-year cycle through 2003 with DRAM capacity accelerated by 1 year.

Table 1 shows target parameters of the SIA roadmap pertaining to digital silicon chip technology. Note the trends in reduction of feature sizes and supply voltages *versus* the increase in chip size, number and density of transistors, and clock frequency. For high-performance devices, this still leads to an increase of power. However, circuits of constant complexity should see a dramatic decrease in power since the projected increase in maximum power is much slower than the increase in maximum complexity.

Technology Choices

Threshold Voltage

For proper functioning of circuits with low supply voltage the threshold voltage must be lowered to about $V_{DD}/2$ and its relative (!) control improved[10]. The analytical expression for the threshold voltage contains a term Q_d/C_{ox}, where Q_d is the charge in the depletion layer and C_{ox} the gate oxide capacitance. Hence, V_t can be lowered by thinning the gate dielectric, increasing its permittivity, and by decreasing the doping. However, short-channel effects, especially punch-through, are usually controlled by *increasing* the channel-doping concentration, thus suppressing the spread of source and drain depletion layers. On the other hand, direct tunneling limits the gate-oxide thickness to about 3 nm.

A solution to this problem has been seen in the use of non-uniform doping. A thin layer of low doping is for the channel followed by wider layer of higher doping. The low-doped zone would reduce V_t as well as increase the mobility through reduced scattering while the high-doped region would suppress short channel effects.[11] Common practice is already the implantation of additional dopants below the channel for threshold control. Ref. [12] gives analytical expressions. Other techniques would involve the epitaxial growth of a low-doped channel layer on a high-doped substrate or the engineering of a retrograde doping profile through implantation.[13] However, suppression of punch-through in deep-submicron devices by the favored latter technique has been questioned by the discovery of a surface punch-through component.[14]

Source and Drain

While the (bulk) punch-through effect demands shallow source/drain junctions, good contacts are more easily achieved through alloying with deeper junctions. Heavy doping of shallow junctions or epitaxial growth have been proposed. Optimization of contact and series resistance as well as punch-through and hot-carrier immunity may be reached by shallow regions with tailored lateral doping profiles. [15]

Table 2 shows SIA's roadmap for doping related solutions.

Leakage

In conventional CMOS processing $S = 100\ mV$ is reached. For $V_t = 0.5\ V$ the subthreshold slope needs to be reduced to $S = 75\ mV$.

Since a MOSFET operating in the subthreshold regime is a “bipolar transistor in disguise”, current flows not only into the drain but also into the bulk. The exponential dependence of the current is in fact caused by the barrier at the source junction.

Another leakage current of interest is the one flowing from source or drain to the bulk. This current is generated in the depletion regions under the junctions by thermal activation of electron-hole pairs, preferentially through midgap traps. It is proportional to the volume of the depletion region and the trap density. These leakage currents play a major role in the charge retention time of DRAM cells.

Two strategies have been proposed to reduce the subthreshold leakage problem:[17]

1. Multiple Threshold Voltages (MTCMOS): Insert transistors with a higher, fixed V_t in series with normal circuitry.
2. Variable Threshold Voltages (VTCMOS): Adjust threshold voltage through substrate bias, either by switching or dynamic adjustment, so that it is high in the quiescent state.

Silicon-On-Insulator (SOI)

The concept of SOI is to place a thin, semiconducting sheet and shallow source/drain regions on an insulating sheet or substrate. The semiconducting sheet, the so-called body, carries the transistor (inversion) channel and can be either partially (PD) or fully depleted (FD) by an isolated gate, like an MOS transistor. Complementary transistors as in CMOS are possible. Fig. 1 shows a schematic cross section. This arrangement solves the aforementioned leakage and threshold problems. It also reduces also all capacitances to ground since this is separated now by the insulating sheet. In addition, due to the complete isolation of transistors, no latch-up or s is possible. Due to the strong coupling of the body to the gate, SOI devices, especially the FD, have superior current on/off ratios, which allows operation at lower supply voltage.

However, since the body is not grounded (unless specifically contacted), its floating causes static and dynamic effects from bipolar currents.[18] These effects diminish the more the body is depleted, i.e., the thinner the body is. Obviously this is more difficult to achieve, and the source/drain regions may not be equally thinned or may be elevated by

250-nm and 180-nm generations, but control of particulate contamination, which leads to pinholes in the BOX, was still a problem.
2. Bonding and etch-back SOI (BESOI): A wafer with the active layer is bonded upside down to a second wafer with the oxide layer. The bulk of the top wafer is then etched away, obviously a formidable task. The formation of a FD device would require a thickness of less than 50 nm.[20]

Table 3 shows SIA's roadmap for SOI *versus* bulk silicon substrate technology.

Figure 2 shows a roadmap for SOI devices in comparison to bulk devices, prepared for NASA's New Millennium Program.[21] Note the steeper learning curve for (Honeywell and Loral) SOI devices, which will meet the bulk DRAM curve around 2004.

Interconnects and Capacitors

Two technological innovations are currently being pursued to reduce power and propagation delay in interconnecting metal lines.[22]

1. Use of copper as interconnect metal: After electro-deposition of copper into dielectric trenches lined with titanium nitride (Damascene Process), the overflowing metal is removed by chemo-mechanical polishing (CMP). This process has the following benefits:

    a. Reduction of sheet resistance through higher conductivity (almost twice that of Al-alloy) and possible larger thickness.
    b. Reduction of wire capacitance to ground due to planarity and higher aspect ratio of wire cross-section.
    c. Larger electromigration lifetime of copper.

2. Use of low-permittivity dielectrics, e.g., porous silicon dioxide (Xerogel). Benefit: Reduces all wire capacitances and with that losses and cross talk.

In the long term, high-temperature superconductors or optical interconnects may be used.

New dielectrics are also pursued for memory storage node and filter capacitors. Here high permittivity and low leakage are desired. Tantalum nitride is a prime candidate.

Table 4 shows SIA's roadmap for interconnect metals and Table 5 that for dielectrics.

Section 3: RF Technology

Currently a large part of mixed signal and RF applications use GaAs because its electron mobility is about 5x that of silicon. Device implementations are the MESFET (Metal Semiconductor Field Effect Transistor), HBT (Heterojunction Bipolar Transistor), and PHEMT (Pseudomorphic High Mobility Transistor), where the latter two types involve one other semiconductor material such as AlAs or InAs.

Market drivers are portable communication devices such as hand-held wireless phones, which work over relay stations, or two-way radios. The ultimate goal for these market would be to produce a "radio on the chip", which integrates RF, digital, and LF functions at low cost. As outlined in the previous Section, digital CMOS silicon technology has nearly reached the communications frequency range of 900 MHz. Functions requiring higher drive currents can be served with BiCMOS, which adds bipolar transistors to the MOSFETs. Moreover, the simplicity of complementary circuits in CMOS can not be matched in the least expensive MESFET GaAs technology.

However, operating CMOS at such high frequencies has its price: It requires high power. Other issues radio-frequency integrated circuits (RFICs) have to consider are noise, linearity, gain, and efficiency.[23] Since mixer conversion efficiency is usually a strong function of the peak drive voltage, it is not expected to see ultra-low voltage supplies as in the digital technology. Typical supply voltage to date is 2.7 V.

A new technology was recently introduced to the commercial RF market using silicon-germanium alloys ($Si_{1-x}\ Ge_x$). These alloys can be epitaxially grown as thin, strained layers on either silicon or germanium with high electron *and* hole mobilities. First commercial applications are Si/ $Si_{1-x}\ Ge_x$/Si HBTs with a base region of graded composition. Another appealing device is a high-mobility p-MOS transistor with a retrograded $Si_{1-x}\ Ge_x$ channel. These devices processed together with normal silicon n-MOS transistors would afford a compact, high-speed, low-power CMOS logic with both types of transistors having the same size. We will report more on SiGe technology in a separate RTOP.

Figure 3 shows the history of transistor cut-off frequencies reported for different technologies[24],[25].

Figure 4 shows an experimental 900 MHz radio on a chip, that is two 1-um bulk CMOS chips [26]. The monolithic transmitter contains "all functions from baseband data (in) to

Tables

Table 1: Selected Target Parameters of SIA Silicon Chip Technology

Year Of First Product Shipment	1997	1999	2001	2003	2006	2009	2012
Dense Lines (DRAM Half–Pitch) (nm)	250	180	150	130	100	70	50
Isolated Lines (MPU Gates) (nm)	200	140	120	100	70	50	35
Chip Size (DRAM) (mm^2)	280	400	445	560	790	1120	1580
Chip Size (MPU) (mm^2)	300	340	385	430	520	620	750
Chip Size (ASIC) (mm^2)	480	800	850	900	1000	1100	1300
Maximum Number of Wiring Levels	6	6–7	7	7	7–8	8–9	9
Memory Capacity @ Introduction (Bit)	256M	1G	1G	4G	16G	64G	256G
Memory Capacity @ Production (Bits)	64M	256M	1G	1G	4G	16G	64G
Memory Density @ Introduction (Bit/cm2)	96M	270M	380M	770M	2.2G	6.1G	17G
Logic (MPU) Density (Transistors/cm^2)	3.7M	6.2M	10M	18M	39M	84M	180M
Logic (ASIC) Density (Transistors/cm^2)	8M	14M	16M	24M	40M	64M	100M
Number of Chip I/Os (High-Performance)	1450	2000	2400	3000	4000	5400	7300
On-Chip Local Clock (High-Perform.) (MHz)	750	1250	1500	2100	3500	6000	10000
Across-Chip Clock (High-Perform.) (MHz)	750	1200	1400	1600	2000	2500	3000

Table 2: Doping Related Potential Solutions (© SEMATECH)

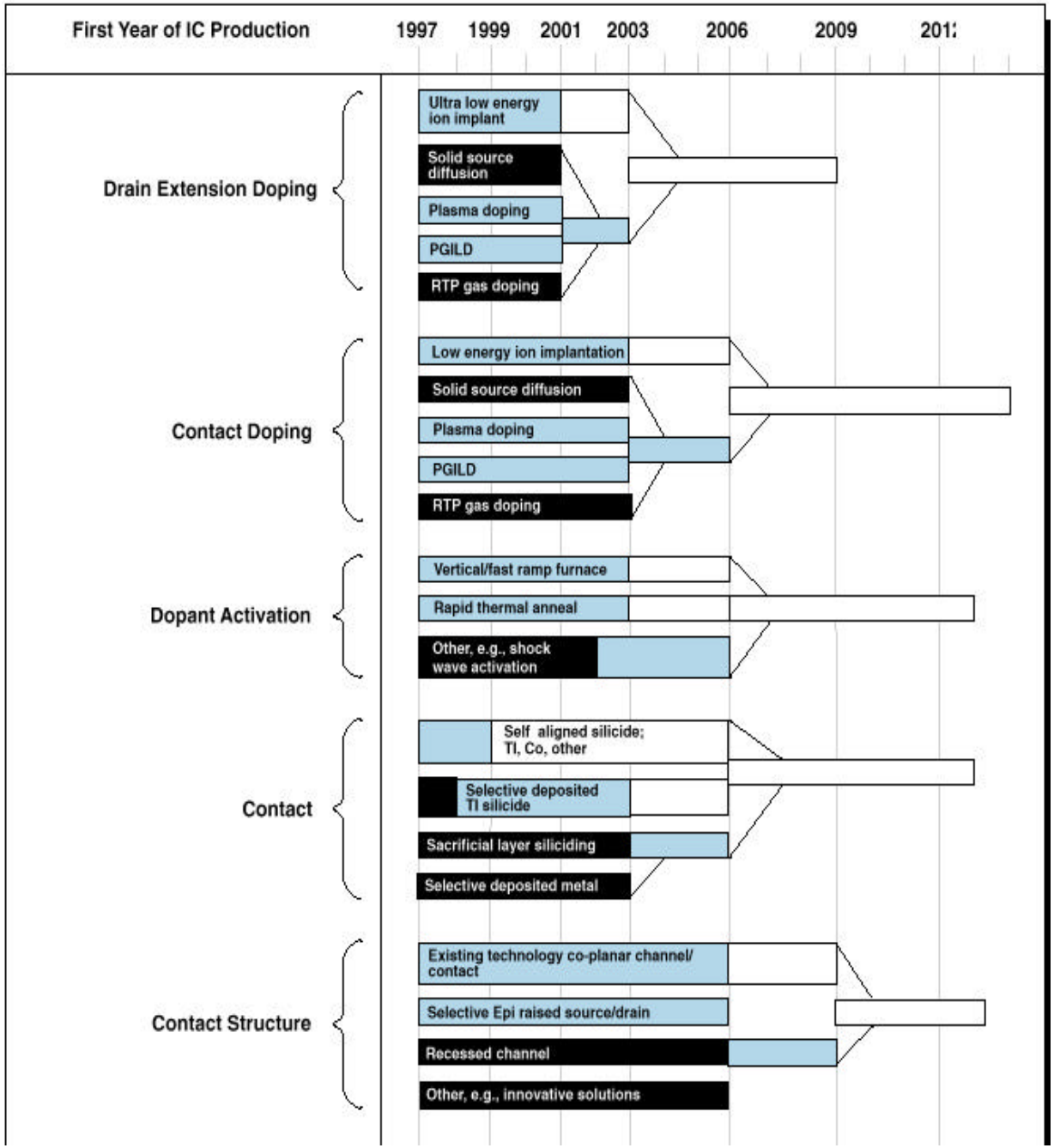


Table 3: Starting Wafers Potential Solutions. Numbers in bars indicate wafer diameter (mm). (© SEMATECH)

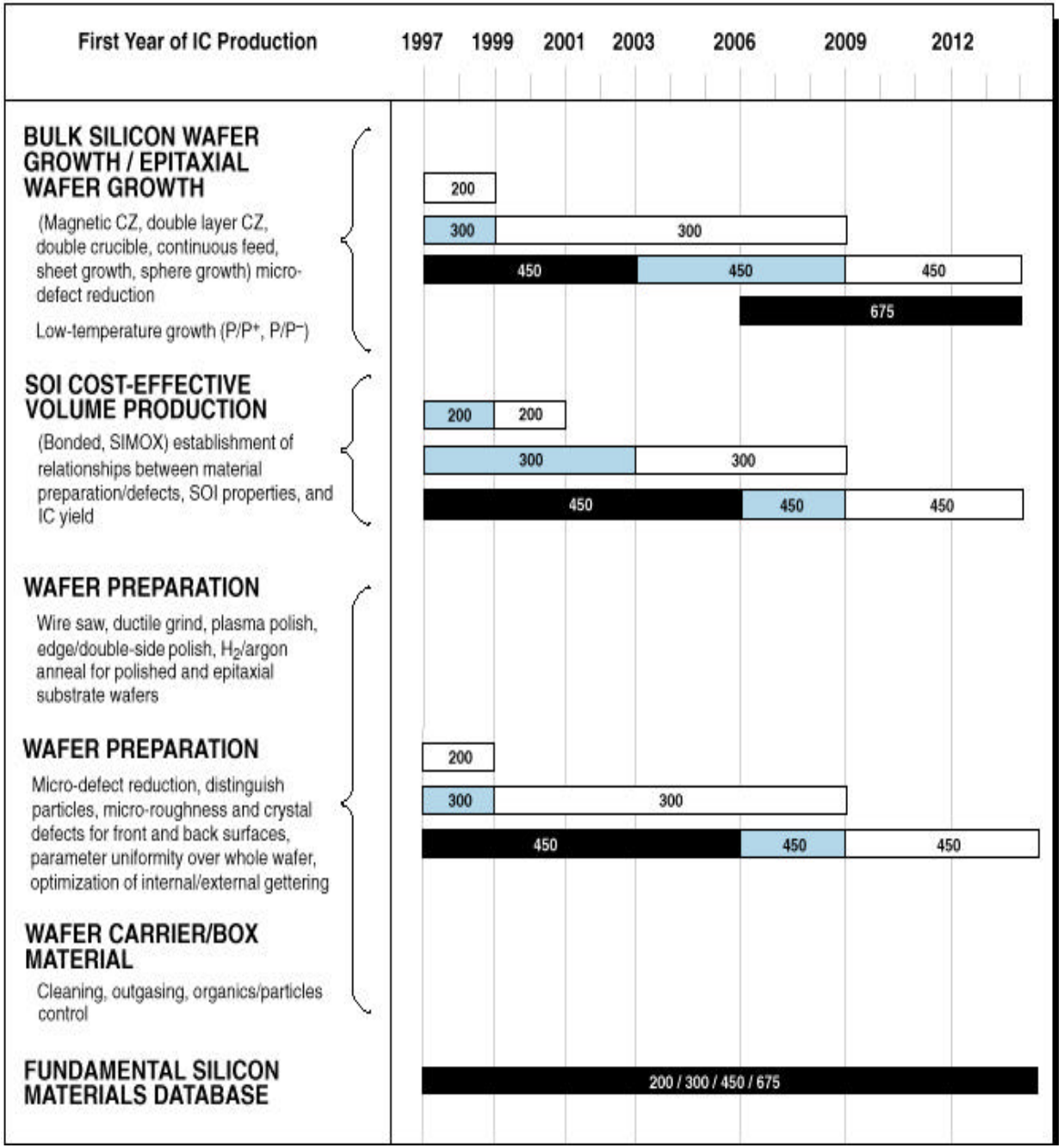


Table 4: Metals Potential Solutions (© SEMATECH)

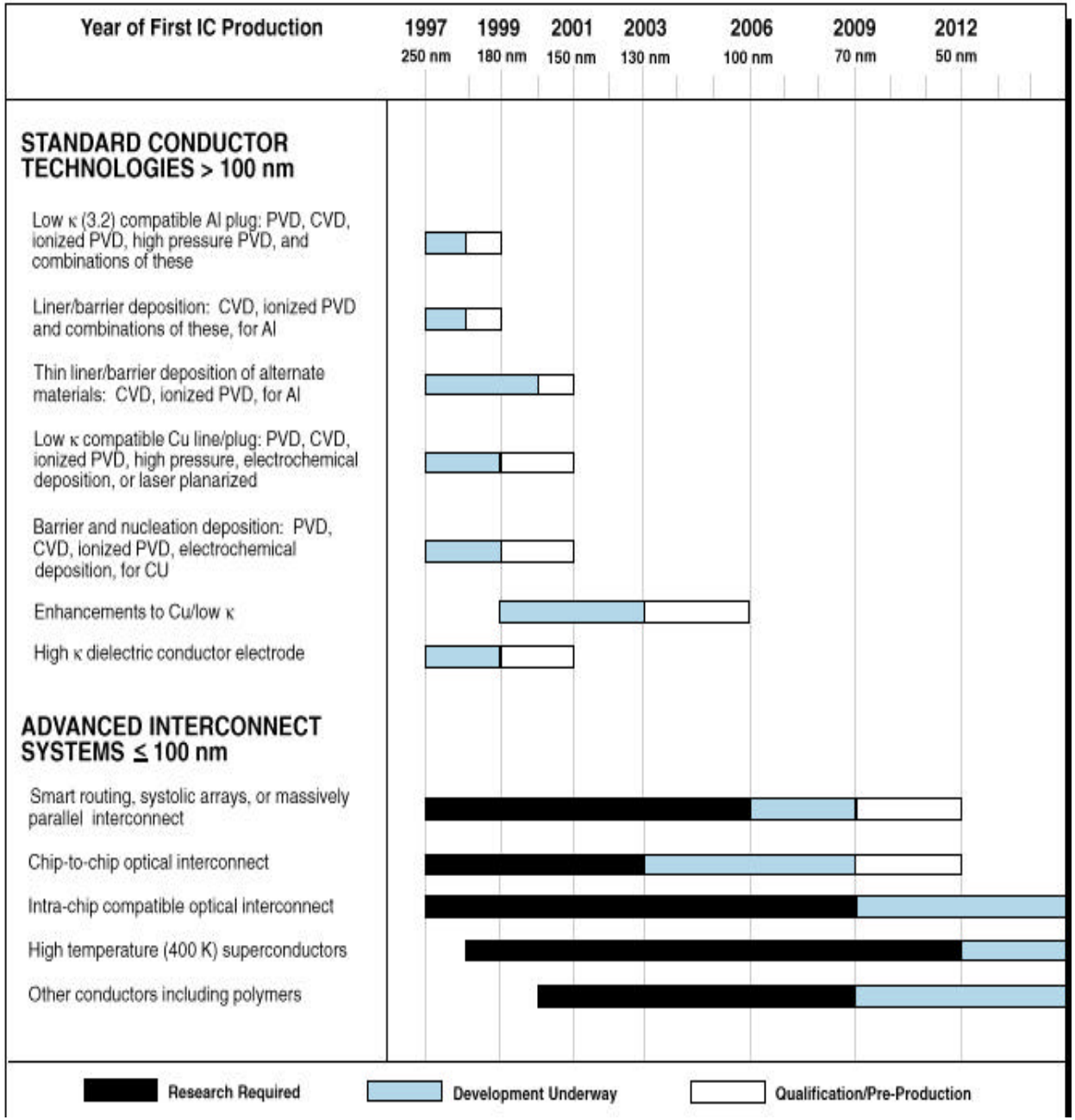
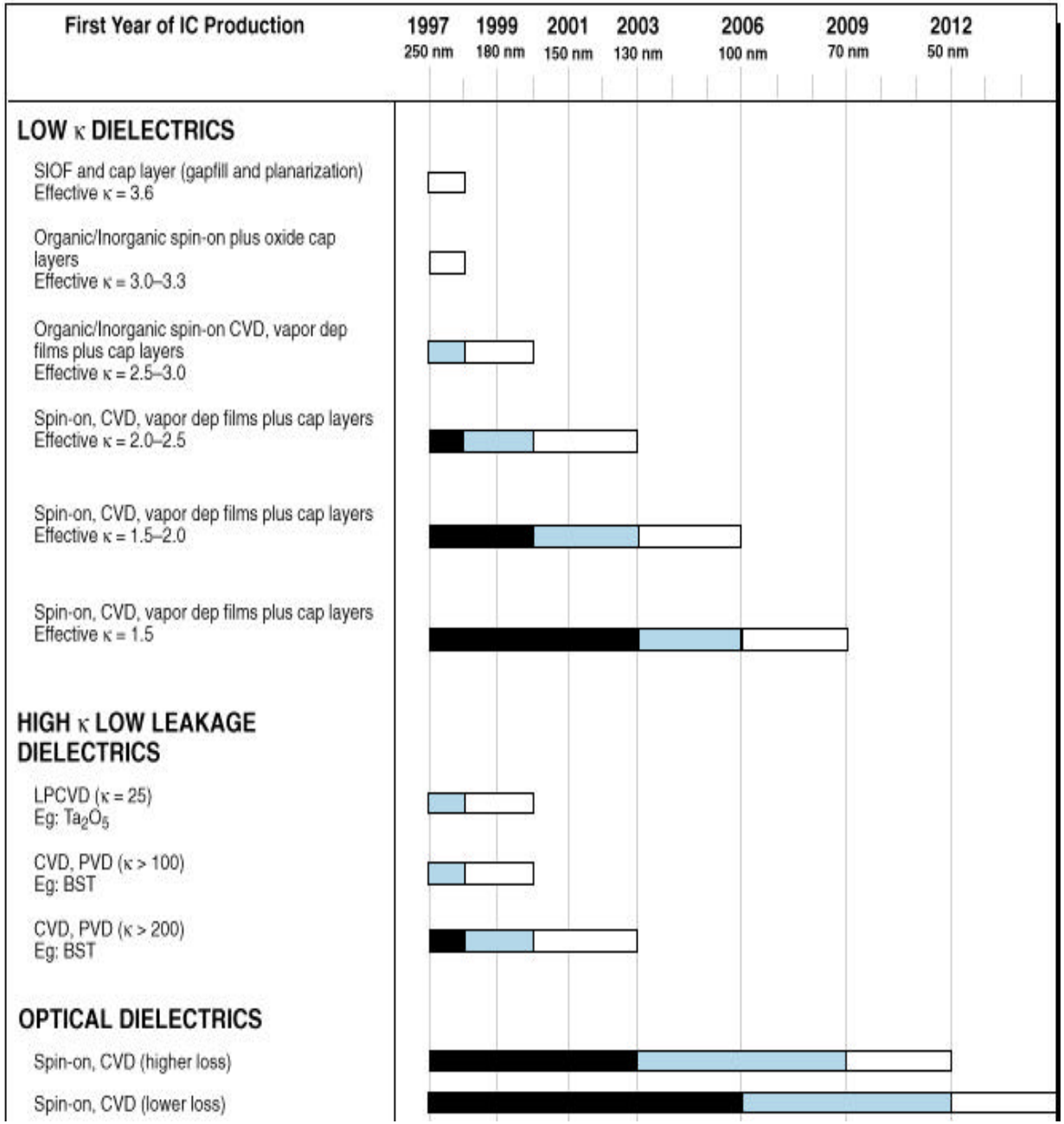


Table 5: Dielectrics Potential Solutions (© SEMATECH)



Figures

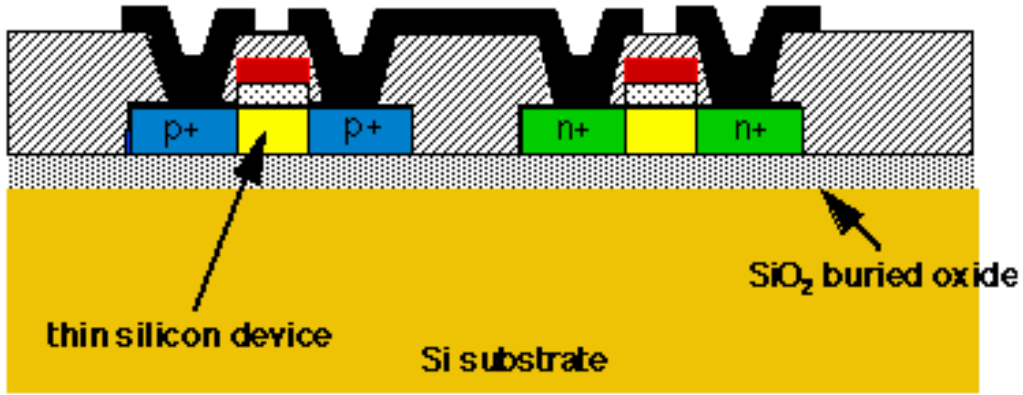


Fig. 1: Silicon-On-Insulator (SOI) cross-section *(schematic)*

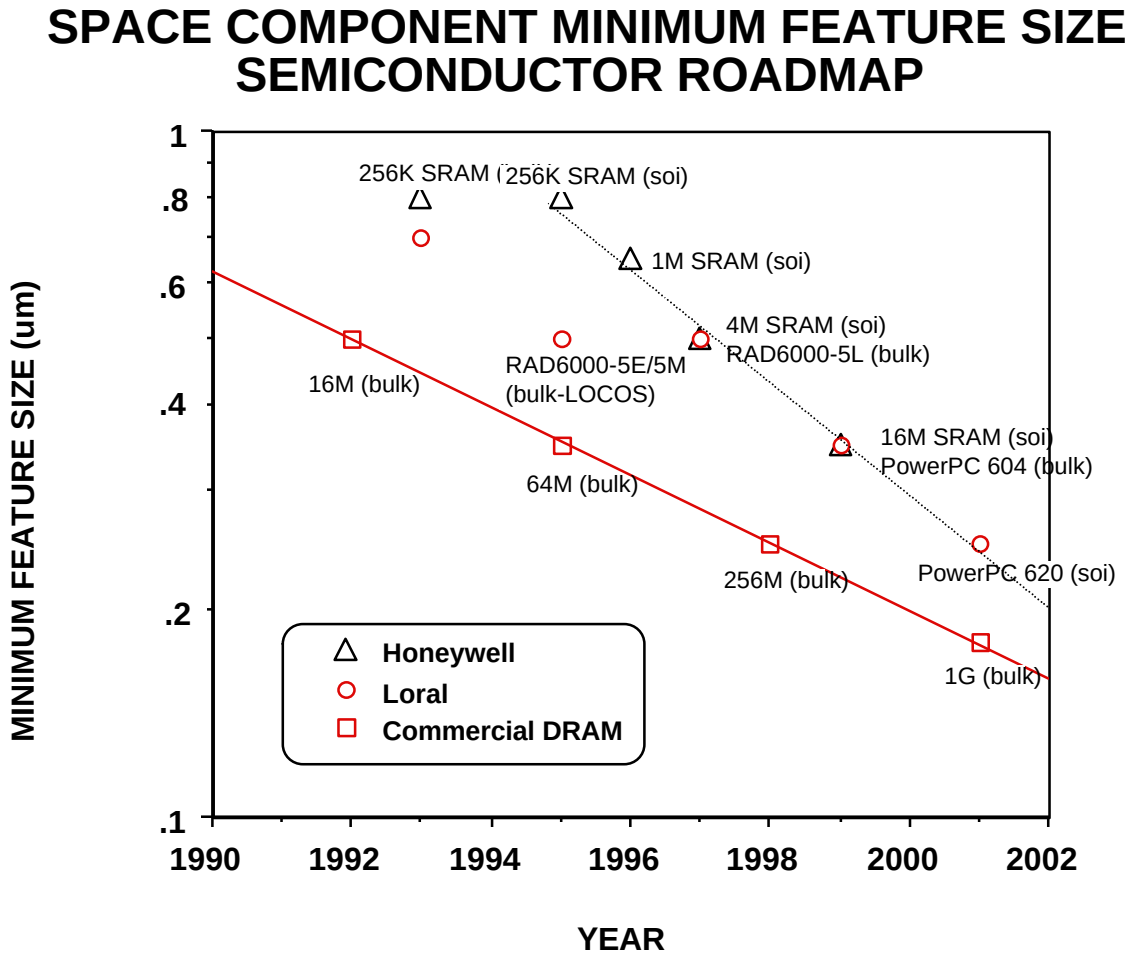


Fig. 2: SOI *vs.* Bulk Silicon Roadmap (New Millennium)

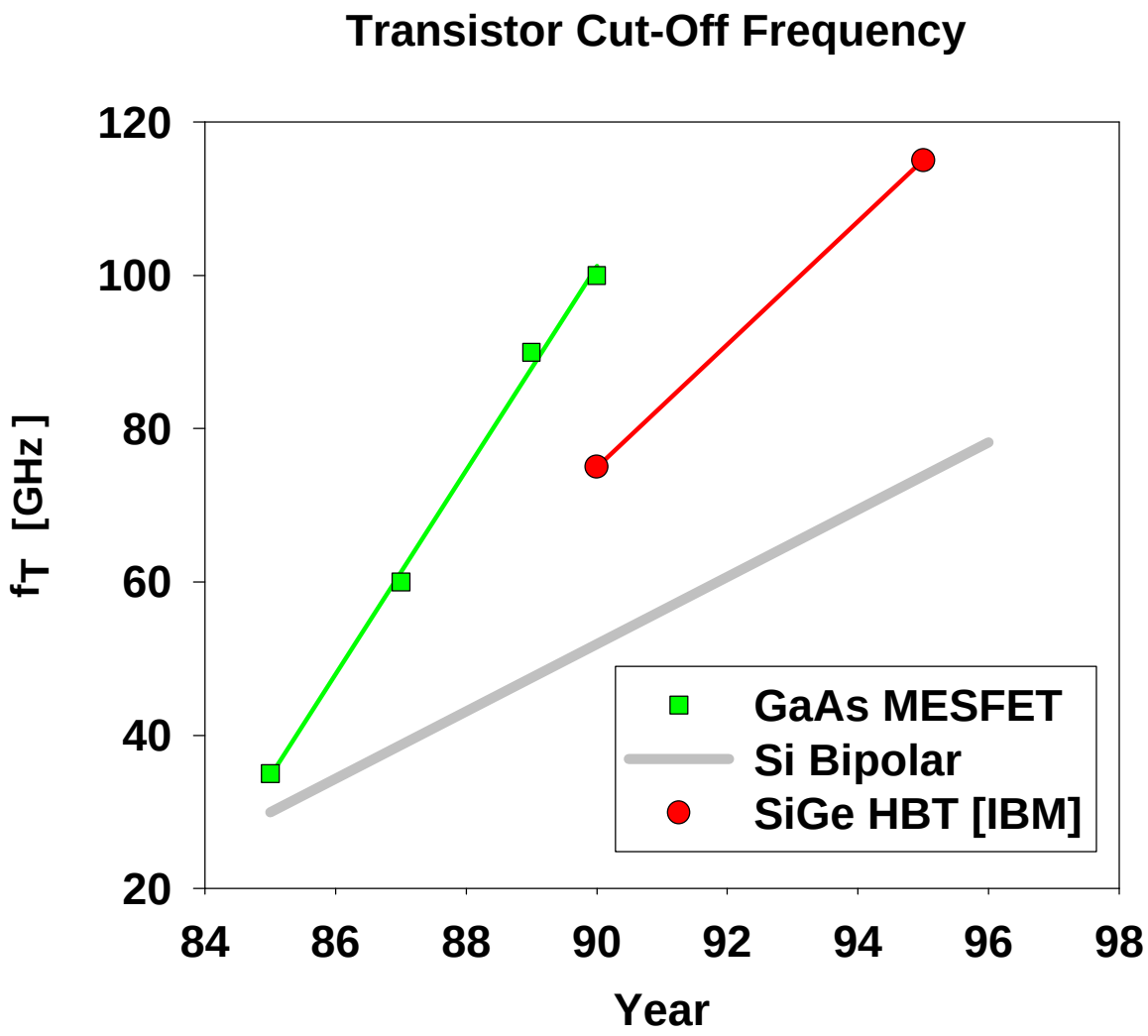
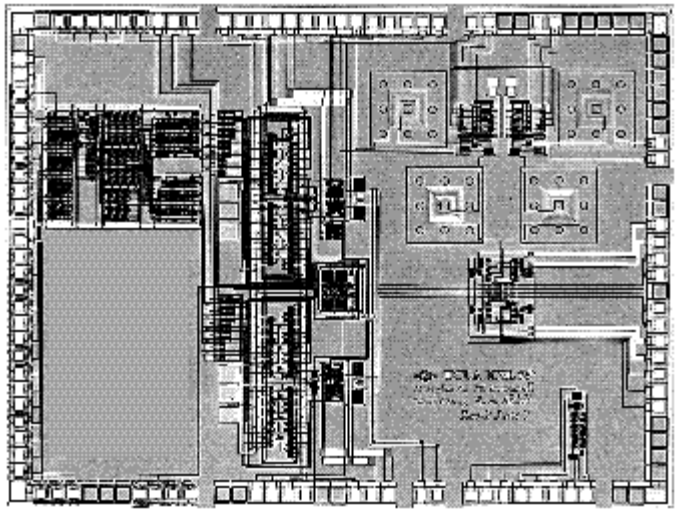
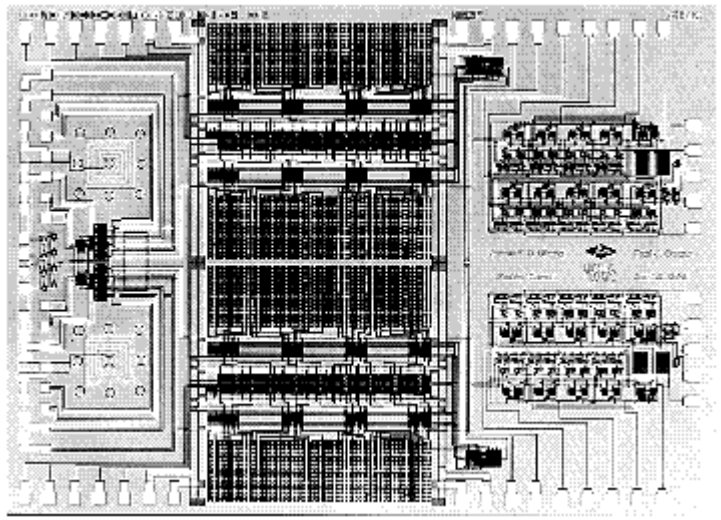


Fig. 3: Transistor cut-off frequency history



(a)



(b)

Fig. 4: Fully integrated 900 MHz transmitter (a) and receiver (b) chips fabricated in 1-um bulk CMOS

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